REMARKS

Reconsideration and allowance of the above-identified application, as currently amended, is respectfully requested.

There are now pending claims 22 through 31 of which claims 22 – 26 and 28 were amended and claims 29 – 31 are newly presented. The amendments made to the claims are inconsideration of further highlighting structurally defining aspects of the set forth semiconductor device including in a manner which better relates the same to the example embodiments in the present application, although not limited thereto.

It is submitted, the set forth semiconductor device as currently defined in claims 22+, 28+ and 31 is, clearly, a patentable improvement over that previously known including over the combined teachings of Lur, et al. (U.S. Patent No. 5,924,006) and Koubuchi, et al. (U.S. Patent No. 6,261,883), as applied in the outstanding rejection under 35 U.S.C. 103(a). Therefore, insofar as presently applicable, this rejection is traversed and reconsideration and withdrawal of the same is respectfully requested.

The invention as now called for in claim 22+, 28+ and 31 is a semiconductor device such as of the type disclosed in the example fifth embodiment of the present application, which is illustrated in Figs. 25 – 27 and described from page 29, paragraph [0110] to page 33, paragraph [0128] of the Specification, although not to be construed as being limited thereto. For example, in Fig. 27 of the drawings, which illustrates a cross-sectional view portion related to a logic integrated circuit device, a dummy wiring system is adapted in accordance with the present invention.

According to the semiconductor device of the present invention, semiconductor elements are formed in the semiconductor substrate, a first interlayer insulation film is formed over the semiconductor elements and first wirings, second wirings and third wirings are formed on the interlayer insulating film, respectively (see independent claim 22). In this regard, the MOSFETs/CMOSFETs which may be formed in the semiconductor substrate 1, relate to the semiconductor elements of the invention as one example thereof, although not limited thereto. Also, the interlayer insulating films such as 10 and 23, although not limited thereto, relate to the set forth "first interlayer insulation film" and the dummy patterns of wirings DML1 and DML2 are example illustrations of the set forth "first wirings" and "second wirings", according to base claim 22, although not limited thereto. According to claim 22, the invention calls for the "third wirings" to be electrically connected with the semiconductor elements and also calls for the first and second wirings to not be electrically connected with the semiconductor elements. An example of the set forth "third wirings" is shown with regard to second layer wirings 24 or, for that matter, first layer wirings 17 while wirings 25 (DML1) and 25 (DML2) are example illustrations of the "first wirings" and "second wirings," respectively. As is shown in Fig. 27, the second layer wirings 24 (or "third wirings" of claim 22) as well as wirings 25 (DML1) and 25 (DML2) are all formed at a same layer and, moreover, it is noted that the claimed "second wirings" are formed regularly and, moreover, the "first wirings" (e.g., DML1) have relatively larger widths and larger planar sizes than that of the second wirings (e.g., DML2), respectively, as shown in the planar view illustration of Fig. 25 of the drawings (see also Figs. 26(a) and 26(b), although not limited thereto.

According to claim 23 (dependent on claim 22), the semiconductor device further calls for a second interlayer insulation film formed on the first, second and third wirings and, moreover, calls for fourth wirings formed on the second interlayer insulation film, wherein the fourth wirings are not electrically connected... and are formed regularly. An example of this can be seen with regard to the patterned wirings 25 which are formed on the interlayer insulating film 23, although not limited thereto. With regard to the examples showings of Fig. 27, although not limited thereto, dummy wirings may also be provided in connection with the process of forming the first layer of wirings 17 or the third layer of wirings 27. Moreover, even when the upper layer wirings are laid on the third layer wirings 27, for example, such dummy wirings can also be provided in the process for forming such wirings (see page 32, paragraph [0122], of the specification, and Figs. 25-27).

The arrangement of the first wirings and second wirings (e.g. DML1 and DML2) in the row direction and/or column direction according to claim 24 are shown, for example, in Fig. 25 of the drawings, although not limited thereto. In accordance with the invention, also, the "second insulation film" is substantially flattened (see page 31, paragraph [0120] and claim 26). Also according to the invention, the wirings may be formed of aluminum or copper (see claim 27 and page 31, paragraph [0119], for example).

The invention according to claims 28+ as well as newly presented independent claim 31 also set forth such featured aspects as the discussed above in connection with claims 22+, although such is presented with some modification therefrom.

It is submitted, the invention according to claims 22+, 28+ and 31 could not have been rendered obvious in view of the combined teachings of Lur, et al. and

Koubuchi, et al. ('883). Lur, et al. employs patterned area 24, which surrounds functional metal lines 20 and 22, as a dummy metal area in connection with achieving planarization (see Figs. 3 and 7). Regarding the scheme taught by Lur, et al., and as shown in Fig. 7 thereof, a capacitance is effected between the metal area 24 and the functional metal lines 40. Such capacitance is present because the metal area 24 covers the entire area except for the portion where the functional metal lines 20 and 22 are present.

Koubuchi, et al. ('883) in Figs. 32-34 thereof, for example, shows a multi-layered interconnection scheme of a semiconductor integrated circuit device. With regard to the plan view illustration in Fig. 34 thereof, it is observed that the dummy interconnections 34 are formed from the same layer as that forming the gate electrode of the MISFET Q1. It is submitted, Koubuchi, et al. ('883) neither shows nor is suggestive of a schemed semiconductor device calling for metal line (wiring) formation and planarized interlayer insulation layer in which different wirings are formed at a same layer which include not only wirings that are electrically connected to semiconductor elements but, also, include "first wirings" and "second wirings" that are not electrically connected and, moreover, are sized relatively differently. In addition to these, there are also other featured aspects contained in claims 22+ and 28+ and, also, in claim 31 (although presented somewhat differently therein) that are not disclosed or suggested from Koubuchi ('883). It is also noted that the pattern dummy interconnections in Koubuchi et al. are similarly shaped and sized. That is, there is neither a showing or suggestion made by Koubuchi et al. of a multi-wiring scheme of a semiconductor device as that presently called for in claims 22+, 28+ and 31 and as discussed hereinabove. It is submitted, also, since Koubuchi, et al., using the Fig. 34 illustration as one example, is not directed to a metal line

scheme (wiring scheme) as that presently called for, but, rather, concerns the formation of dummy interconnections, one of ordinary skill would not have been motivated to combine the teachings of Koubuchi, et al. ('883) and Lur et al. Therefore, for at least the above reasons, the invention according to claims 22+, 28+ and 31 could not have been rendered obvious in the manner alleged over the combination of Lur et al. and Koubuchi et al. ('883).

As to the previously standing rejection of claim 1, "under the judicially created doctrine of obviousness-type double patenting" over the claimed disclosure of prior U.S. Patent No. 6,693,315, it has been rendered moot with the canceling of this claim. It is submitted, however, agree to the canceling of this claim should not construed as acquiescence with regard to the merits of the rejection directed thereto.

Therefore, in view of the above made amendments together with these accompanying remarks, reconsideration and withdrawal of the outstanding rejections as well as favorable action on the currently pending claims, i.e., claims 22-31, and an early formal notification of allowance of the above-identified application is respectfully requested.

If the Examiner deems that questions and/or issues still remain which would prevent the present application from being allowed at the present time, he/she is invited to telephone the undersigned representative, at the telephone number indicated below, so that either a telephone or personal interview may be arranged at the Examiner's convenience in order to discuss the same and hopefully resolve any remaining questions/issues present.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the

filing of this paper, including Extension of Time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (501.40803VX1), and please credit any excess fees to such deposit account.

Respectfully submitted,
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